Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**\*DO NOT BOND TO CENTER AREA\***

**.025”**

**.025”**

**NO**

**BOND**

**.019”**

**BOND**

**PAD**

**ANODE**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .019” X .019” (See Above)**

**Backside Potential: Collector**

**Mask Ref: ZAA**

**APPROVED BY: DK DIE SIZE .025” X .025” DATE: 8/31/21**

**MFG: ALLEGRO / SPRAGUE THICKNESS .010” P/N: 1 N750A**

**DG 10.1.2**

#### Rev B, 7/19/02